

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: David J. Corisis

Patent No.: 6,977,214 B2

Issued: December 20, 2005

For: DIE PADDLE CLAMPING METHOD
FOR WIRE BOND ENHANCEMENT

Attorney Docket No.: 2269-3388.6

VIA ELECTRONIC FILING

October 5, 2007

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR APPLICANT MISTAKES (37 C.F.R. § 1.323) AND
PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)**

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that a combination of Applicant and Patent Office errors appear in this patent of a typographical nature or character and correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination. A certificate of correction in the form attached hereto is requested.

Please send the Certificate to:

Name: James R. Duzan
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

Please note that an Amendment Pursuant to 37 C.F.R. § 1.312(a) (copy enclosed) was filed concurrently with the issue fee on September 30, 2005, but the amendments contained

therein were apparently not completely included in the printed patent. Attached is a copy of the previously filed Amendment Pursuant to 37 C.F.R. § 1.312(a) and the date-stamped postcard, acknowledging receipt by the PTO, to provide proof of such filing. The subject matter of this amendment is included in the attached Certificate of Correction.

The Commissioner is authorized to charge \$100.00 to the TraskBritt Deposit Account No. 20-1469 for the fee as required by 37 C.F.R. § 1.20(a).

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: October 5, 2007
JRD/dflh

Attachment: PTO/SB/44
copy of Amendment Pursuant to 37 C.F.R. § 1.312(a)
copy of date-stamped postcard

Document in ProLaw

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 6,977,214 B2
APPLICATION NO. : 09/943,763
ISSUE DATE : December 20, 2005
INVENTOR(S) : David J. Corisis

Page 1 of 5

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page:

In column 2 below (57) **ABSTRACT** change "28 Claims, 4 Drawing Sheets" to --27 Claims, 4 Drawing Sheets--

In the drawings:

In FIG. 3, replace informal drawing of FIG. 3 with formal drawing of FIG. 3
In FIG. 4, replace informal drawing of FIG. 4 with formal drawing of FIG. 4
In FIG. 5, replace informal drawing of FIG. 5 with formal drawing of FIG. 5

In the specification:

COLUMN 3, LINE 17, after "on" and before "leadframe" insert --the--
COLUMN 3, LINES 21-22, delete "These tabs may be formed on the sides of the paddle along which from the paddle support bars."

In the claims:

CLAIM 1, COLUMN 6, LINE 15, change "arid" to --and--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

James R. Duzan
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 6,977,214 B2
APPLICATION NO : 09/943,763
ISSUE DATE : December 20, 2005
INVENTOR(S) : David J. Corisis

Page 2 of 5

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 28, COLUMN 12, LINES 13-25, delete "28. A method of bonding a portion of a wire to a portion of a lead of a leadframe having a semiconductor device having a plurality of bond pads attached to a portion of a die mount paddle of a leadframe, said method comprising:
locating said strip of leadframes on a lower clamp member of a wire bonding device having an upper clamp member overlying a portion of at least one lead and a portion of at least one integral clamping tab of said strip of leadframes; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads."

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230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,977,214 B2
 APPLICATION NO. : 09/943,763
 ISSUE DATE : December 20, 2005
 INVENTOR(S) : David J. Corisis

Page 3 of 5

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace FIG. 3 with the following amended figure:

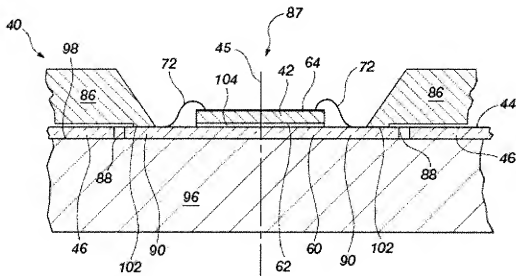


Fig. 3

MAILING ADDRESS OF SENDER (Please do not use customer number below):

James R. Duzan
 TRASKBRIIT
 230 South 500 East, Suite 300
 Salt Lake City, Utah 84102 USA

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

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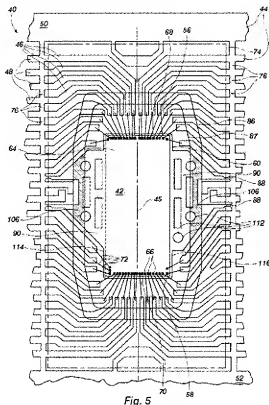
UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 6,977,214 B2
APPLICATION NO. : 09/943,763
ISSUE DATE : December 20, 2005
INVENTOR(S) : David J. Corisis

Page 5 of 5

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace FIG. 5 with the following amended figure:



MAILING ADDRESS OF SENDER (Please do not use customer number below):

James R. Duzan
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230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

David J. Corisis

Serial No.: 09/943,763

Filed: August 30, 2001

For: DIE PADDLE CLAMPING METHOD
FOR WIRE BOND ENHANCEMENT

Confirmation No.: 2592

Examiner: J. Mitchell

Group Art Unit: 2813

Attorney Docket No.: 2269-3388.6US
(97-0560.05/US)

Notice of Allowance Mailed:

July 1, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL955991197US

Date of Deposit with USPS: September 30, 2005

Person making Deposit: Steve Wong

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Specification appear on page 3 of this paper.

Serial No. 09/943,763

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 15 of this paper.

IN THE SPECIFICATION:

Please amend paragraph number [0001] as follows:

[0001] This application is a continuation of application Serial No. 09/635,023, filed August 4, 2000, ~~pending, now U.S. Patent 6,326,238, issued December 4, 2001,~~ which is a continuation of application Serial No. 09/210,013 filed December 11, 1998, now U.S. Patent 6,162,662, issued December 19, 2000.

Please amend paragraph number [0008] as follows:

[0008] During semiconductor die attach and wire bonding, the inner leads are typically clamped against a lower heater block or other flat member. The bonding tool itself is configured to compress the wire against the surface to which the wire is being bonded, i.e., a bond pad or inner lead. Examples of such are found in United States Patent 4,600,138 of Hill, United States Patent 4,030,657 of Scheffer, United States Patent 4,603,803 of Chan et al., United States Patent 4,778,097 of Hauser, United States Patent 5,148,959 of Cain et al., United States Patent 5,217,154 of Elwood et al., United States Patent 5,421,503 of Perlberg et al., and United States Patent 5,445,306 of Huddleston. It has generally been found, however, that auxiliary clamping apparatus may improve the quality of "~~second-bonding~~", bonding," i.e., bonding of the wire to the inner leads.

IN THE CLAIMS:

Please cancel Claim 28 herein. Claims 1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 16, 18, 19, 21, 22, 24, 25, and 27 have been amended herein. All of the pending claims 1 through 27 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) An assembly method for a semiconductor device assembly using a wire bonding device having an upper clamp member and a lower clamp member, said method comprising:
providing at least a portion of a strip of ~~lead frames~~, leadframes, said strip having opposed rails, having dam bars between said opposed rails, having at least two inner leads located at a first level, having at least two outer leads located at a second level, having a die mount paddle located at a third level and having at least one integral clamping tab, said at least one integral clamping tab located at a fourth level extending outwardly for contact by said upper clamp member;
attaching a semiconductor device to said die mount paddle, said semiconductor device having a plurality of bond pads;
locating said strip of ~~lead frames~~, leadframes on said lower clamp member of said wire bonding device having said upper clamp member overlying portions of said at least two inner leads and portions of said at least one integral clamping tab; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads.

2. (Previously presented) The method of claim 1, further comprising:
forming said die mount paddle having an upper surface thereof at a third level located below an upper first level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

3. (Currently amended) The method of claim 1, further comprising:
removing said strip of ~~lead frames~~ leadframes and said semiconductor device from said lower clamp member; and
encapsulating a portion of said strip of ~~lead frames~~ leadframes, said semiconductor device, and said at least two bond wires extending between said strip of ~~lead frames~~ leadframes and said semiconductor device in a material.

4. (Currently amended) A method for assembling a semiconductor device assembly having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding device having an upper clamp member and a lower clamp member, said method comprising:
supplying at least a portion of a strip of ~~lead frames~~ leadframes, said strip having opposed rails, having dam bars between said opposed rails, having at least two inner leads located at a first vertical level, having at least two outer leads located at a second vertical level, having a die mount paddle located at a third vertical level and having at least one integral clamping tab, said at least one integral clamping tab located at a fourth vertical level extending outwardly for contact by said upper clamp member;
attaching a semiconductor device to said die mount paddle, said semiconductor device having a plurality of bond pads;
locating at least a portion said strip of ~~lead frames~~ leadframes on said lower clamp member of said wire bonding device having said upper clamp member overlying portions of said at least two inner leads and portions of said at least one integral clamping tab; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads.

5. (Previously presented) The method of claim 4, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

6. (Currently amended) The method of claim 4, further comprising:
removing said strip of ~~lead frames~~ leadframes and said semiconductor device from said lower clamp member; and
encapsulating a portion of said strip of ~~lead frames~~ leadframes, said semiconductor device, and
~~said~~ at least two bond wires extending between said strip of ~~lead frames~~ leadframes and
said semiconductor device in a material.

7. (Currently amended) A method for assembling a semiconductor device assembly having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding device having an upper clamp member and a lower clamp member, said method comprising:
providing at least a portion of a strip of ~~lead frames~~ leadframes, said strip having opposed rails,
having dam bars between said opposed rails, having at least two inner leads located at a first vertical level, having at least two outer leads located at a second vertical level,
having a die mount paddle located at a third vertical level and having at least one integral clamping tab, said at least one integral clamping tab located at a fourth vertical level extending outwardly for contact by said upper clamp member, said die mount paddle having a semiconductor device attached thereto, said semiconductor device having a plurality of bond pads;
locating at least a portion of said strip of ~~lead frames~~ leadframes on said lower clamp member of said wire bonding device having said upper clamp member overlying portions of said at least two inner leads and portions of said at least one integral clamping tab;

clamping portions of said ~~lead frame~~ leadframe using said upper clamp contacting portions of said ~~lead frame~~ leadframe while portions of said lower clamp contact portions of said ~~lead frame~~ leadframe; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads.

8. (Previously presented) The method of claim 7, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

9. (Currently amended) The method of claim 7, further comprising:
removing said strip of ~~lead frames~~ leadframes and said semiconductor device from said lower clamp member; and
encapsulating a portion of said strip of ~~lead frames~~ leadframes, said semiconductor device, and said at least two bond wires extending between said strip of ~~lead frames~~ leadframes and said semiconductor device in a material.

10. (Currently amended) A method for assembling a semiconductor device assembly having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding device having an upper clamp member and a lower clamp member, said method comprising: supplying a portion of a strip of ~~lead frames~~ leadframes, said strip having opposed rails, having dam bars between said opposed rails, having at least two inner leads located at a first vertical level, having at least two outer leads located at a second ~~vertical~~ vertical level, having a die mount paddle located at a third vertical level and having at least one integral clamping tab, said at least one integral clamping tab located at a fourth vertical level extending outwardly for contact by said upper clamp member, said die mount paddle having a semiconductor device attached thereto, said semiconductor device having a plurality bond pads;

locating at least a portion of said strip of ~~lead frames~~ leadframes on said lower clamp member of said wire bonding device having said upper clamp member overlying portions of said at least two inner leads and portions of said at least one integral clamping tab; and attaching at least one bond wire to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads.

11. (Previously presented) The method of claim 10, further comprising:

forming said die mount paddle having an upper surface thereof at a third vertical level located below an upper first vertical level of said at least two inner leads; and

deforming said at least one integral clamping tab to clamp portions thereof.

12. (Currently amended) The method of claim 10, further comprising:
removing said strip of ~~lead frames~~ leadframes and said semiconductor device from said lower
clamp member; and
encapsulating a portion of said strip of ~~lead frames~~ leadframes, said semiconductor device, and
~~said at least two bond wires extending between said strip of lead frames~~ leadframes and
said semiconductor device in a material.

13. (Currently amended) A method for assembling a semiconductor device assembly
having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding
device having an upper clamp member and a lower clamp member, said method comprising:
supplying a portion of a strip of ~~lead frames~~ leadframes, said strip having opposed rails, having
dam bars between said opposed rails, having at least two inner leads located at a first
level, having at least two outer leads located at a second level, having a die mount paddle
located at a third level and having at least one integral clamping tab, said at least one
integral clamping tab located at a fourth level extending outwardly for contact by said
upper clamp member, said die mount paddle having a semiconductor device attached
thereto, said semiconductor device having a plurality of bond pads;
locating at least a portion of said strip of ~~lead frames~~ leadframes on said lower clamp member
of said wire bonding device having said upper clamp member overlying portions of said
at least two inner leads and portions of said at least one integral clamping tab;
preventing substantial movement of said die mount paddle by clamping a portion thereof; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and
said portions of said at least two inner leads.

14. (Previously presented) The method of claim 13, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located
below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

15. (Currently amended) The method of claim 13, further comprising:
removing said strip of ~~lead frames~~ leadframes and said semiconductor device from said lower
clamp member; and
encapsulating a portion of said strip of ~~lead frames~~ leadframes, said semiconductor device, and
~~said~~ at least two bond wires extending between said strip of ~~lead frames~~ leadframes and
said semiconductor device in a material.

16. (Currently amended) A method for assembling a semiconductor device assembly
having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding
device having an upper clamp member and a lower clamp member, said method comprising:
supplying at least a portion of a strip of ~~lead frames~~ leadframes, said strip having opposed rails,
having dam bars between said opposed rails, having at least two inner leads located at a
first level, having at least two outer leads located at a second level, having a die mount
paddle located at a third level and having at least one integral clamping tab, said at least
one integral clamping tab located at a fourth level extending outwardly for contact by said
upper clamp member, said die mount paddle having a semiconductor device attached
thereto, said semiconductor device having a plurality of bond pads;
locating at least a portion of said strip of ~~lead frames~~ leadframes on said lower clamp member
of said wire bonding device having said upper clamp member overlying portions of said
at least two inner leads and portions of said at least one integral clamping tab;
forcing portions of said die mount paddle into contact with portions of said lower clamp; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and
said portions of said at least two inner leads.

17. (Previously presented) The method of claim 16, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located
below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

18. (Currently amended) The method of claim 16, further comprising:
removing said strip of ~~lead frames~~ leadframes and said semiconductor device from said lower
clamp member; and
encapsulating a portion of said strip of ~~lead frames~~ leadframes, said semiconductor device, and
~~said at least two bond wires extending between said strip of lead frames~~ leadframes and
said semiconductor device in a material.

19. (Currently amended) A method for assembling a semiconductor device assembly
having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding
device having an upper clamp member and a lower clamp member, said method comprising:
supplying at least one ~~lead frame~~ leadframe from a strip of ~~lead frames~~ leadframes having
opposed rails, having dam bars between said opposed rails, having at least two inner leads
located at a first level, having at least two outer leads located at a second level, having a
die mount paddle located at a third level and having at least one integral clamping tab,
said at least one integral clamping tab located at a fourth level extending outwardly for
contact by said upper clamp member, said die mount paddle having a semiconductor
device attached thereto, said semiconductor device having a plurality of bond pads;
locating at least a portion of said at least one ~~lead frame~~ leadframe on said lower clamp member
of said wire bonding device having said upper clamp member overlying portions of said
at least two inner leads and portions of said at least one integral clamping tab;
forcing portions of said die mount paddle into contact with portions of said lower clamp; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and
said portions of said at least two inner leads.

20. (Previously presented) The method of claim 19, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located
below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

21. (Currently amended) The method of claim 19, further comprising:
removing said at least one ~~lead frame~~ leadframe and said semiconductor device from said lower
clamp member; and
encapsulating a portion of said at least one ~~lead frame~~ leadframe, said semiconductor device,
and said at least two bond wires extending between said strip of ~~lead frames~~ leadframes
and said semiconductor device in a material.

22. (Currently amended) A method for assembling a semiconductor device assembly
having a semiconductor device and portions of a ~~lead frame~~ leadframe using a wire bonding
device having an upper clamp member and a lower clamp member, said method comprising:
supplying at least one ~~lead frame~~ leadframe from a strip of ~~lead frames~~ leadframes having
opposed rails, having dam bars between said opposed rails, having at least two inner leads
located at a first level, having at least two outer leads located at a second level, having a
die mount paddle located at a third level and having at least one integral clamping tab,
said at least one integral clamping tab located at a fourth level extending outwardly for
contact by said upper clamp member, said die mount paddle having a semiconductor
device attached thereto, said semiconductor device having a plurality of bond pads;
locating at least a portion of said at least one ~~lead frame~~ leadframe on said lower clamp member
of said wire bonding device having said upper clamp member overlying portions of said
at least two inner leads and portions of said at least one integral clamping tab;
preventing substantial movement of portions of said die mount paddle by contacting portions of
said die mount paddle with said upper clamp and said lower clamp; and
attaching at least one bond wire to said plurality of bond pads of said semiconductor device and
said portions of said at least two inner leads.

23. (Previously presented) The method of claim 22, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located
below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

24. (Currently amended) The method of claim 22, further comprising:
removing said strip of ~~lead-frames~~ leadframes and said semiconductor device from said lower
clamp member; and
encapsulating a portion of said at least one ~~lead-frame~~ leadframe from a strip of ~~lead-frames~~,
leadframes, said semiconductor device, and said at least two bond wires extending
between at least one ~~lead-frame~~ leadframe from a strip of ~~lead-frames~~ leadframes and
said semiconductor device in a material.

25. (Currently amended) A method for assembling a semiconductor device assembly
having a semiconductor device and portions of a ~~lead-frame~~ leadframe using a wire bonding
device having an upper clamp member and a lower clamp member, said method comprising:
supplying at least one ~~lead-frame~~ leadframe from a strip of ~~lead-frames~~, leadframes, said strip
having opposed rails, having dam bars between said opposed rails, having at least two
inner leads, having at least two outer leads, having a die mount paddle located and having
at least one integral clamping tab, said at least one integral clamping tab extending
outwardly for contact by said upper clamp member, said die mount paddle having a
semiconductor device attached thereto, said semiconductor device having a plurality of
bond pads;
locating at least a portion of said strip of ~~lead-frames~~ leadframes on said lower clamp member
of said wire bonding device having said upper clamp member overlying portions of said
at least two inner leads and portions of said at least one integral clamping tab;

forcing portions of said die mount paddle into contact with portions of said lower clamp; and attaching at least one bond wire to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads.

26. (Previously presented) The method of claim 25, further comprising:
forming said die mount paddle having an upper surface thereof at a third vertical level located below an upper first vertical level of said at least two inner leads; and
deforming said at least one integral clamping tab to clamp portions thereof.

27. (Currently amended) The method of claim 25, further comprising:
removing said at least one ~~lead frame~~ leadframe from a strip of ~~lead frames~~ leadframes and said semiconductor device from said lower clamp member; and
encapsulating a portion of said ~~lead frame~~ leadframe from a strip of ~~lead frames~~ leadframes, said semiconductor device, and said at least two bond wires extending between said at least one ~~lead frame~~ leadframe from said strip of ~~lead frames~~ leadframes and said semiconductor device in a material.

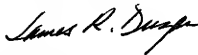
28. (Cancelled)

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
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P.O. Box 2550
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Telephone: 801-532-1922

Date: September 30, 2005
JRD/csw

THE PATENT & TRADEMARK OFFICE MAILROOM DATE
STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THIS
DATE THIS PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Letter (2 pages, w/duplicate copy); Part B - Issue Fee
Transmittal (1 page, w/duplicate copy); Check No. 22:70 in the amount of
\$1,715.00; Amendment Pursuant to 37 C.F.R. § 1.312(a) (15 pages);
Comments on Statement of Reasons for Allowance (2 pages); and Fee
Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2
pages).

Invention: DIE PADDLE CLAMPING METHOD FOR WIRE
BOND ENHANCEMENT

Applicant(s): David J. Corisis

Filing Date: August 30, 2001

Serial No.: 09/943,763

Date Sent: September 30, 2005 via Express Mail 1
EL995991197US

Docket No.: 2269-3388.6US

JRD/dlm:lmh

RECEIVED

OCT 16 2005

TRASSL BRITT, PC.

